European Innovation Council

CHALLENGE GUIDE

PATHFINDER CHALLENGE: Nanoelectronics for energy-efficient smart edge devices

EIC Work Programme reference: HORIZON-EIC-2024-PATHFINDERCHALLENGES-04
Call deadline date: 16 October 2024
EIC Programme Manager: Isabel Obieta

The EIC will hold an Info Session on this Pathfinder Challenge call on March 20, 2024, between 09:00 and 13:00 CET. Participants can access the meeting as guests at https://webcast.ec.europa.eu/information-day-eic-work-programme-2024-pathfinder-challenges-2024-03-20.
Participation in the meeting, although encouraged, is optional and is not required for the submission of an application. A recording of this Info Session will be made available on the same URL. Notifications of additional dissemination events can be found at https://eic.ec.europa.eu/events/save-date-european-innovation-council-pathfinder-challenges-work-programme-2024-info-day-2024-03-20_en.

Table of Contents

1 About this document

The Challenge Guide serves as guidance and background for the common understanding, participation rules and obligations for the EIC beneficiaries that are involved in the Challenge Portfolio. Contractual Obligations are further detailed in the EIC Work Programme 2024 https://eic.ec.europa.eu/system/files/2023-12/EIC-workprogramme-2024.pdf

The Challenge Guide is a guidance document accompanying a Pathfinder Challenge call for proposals to provide further information about how "Portfolio Considerations" will be taken into account in the evaluation of proposals.

The Challenge Guide is prepared by and under the responsibility of the relevant EIC Programme Manager (information about the EIC Programme Managers is available on the EIC Website https://eic.ec.europa.eu/eic-communities/eic-programme-managers_en). It complements the Scope, Specific Objectives and/or Specific Conditions set out in the EIC Work Programme by a description of the portfolio considerations and how a portfolio will be built. The presentation provided by the Programme Manager during the Info Day will give applicants a further opportunity to understand the background of the call, and to ask questions to the Programme Manager. In no case does the Challenge Guide contradict or supplant the Work Programme text.

Following the selection of a proposal to be funded under the Challenge, the Programme Manager will work together with the consortia of the selected projects to develop a common roadmap with a strategic plan for the Challenge. This roadmap/ strategy plan will integrate the activities and milestones of the individual projects into a shared set of objectives and activities across and beyond the projects. The roadmap serves as a common basis for the project portfolio and may affect the project implementation - including possible adjustments, reorientations, or additional support to projects. The roadmap will be updated in light of emerging results or issues during the implementation.

2 The scope and objectives of the Challenge as defined in the Work Programme

This section is a copy of the Challenge call in the EIC Work Programme text. Proposals to this Challenge are expected to explain how they relate to and intend to go beyond the state of the art, and how they interpret and contribute to the objectives of the Challenge.

2.1 Background and scope

Power consumption and heat dissipation are the most urgent challenges in electronics ranging from mobile devices to large data centres and becomes especially relevant for smart

edge devices. Advanced chip designs are lowering energy consumption of microelectronic components, devices, and systems, while increasing performance such as speed, capacity, reliability and security. Applications include artificial intelligence, communications, computing and sensing.
Various strategies are and have been tested, but still there is much room to improve power consumption towards near-fundamental limits, through the co-design of geometry, materials, circuits, and integration in a holistic approach.
The overall goal of this challenge is to explore novel materials and beyond CMOS devices, non-von Neumann architectures and alternative information processing paradigms to drastically reduce energy consumption in order to meet application-specific needs of smart edge devices and circuits.

2.2 Specific objectives

The overall objective of this challenge is to explore solutions (starting at TRL 1/2) that will have a drastic impact on decreasing the energy consumption of any smart edge device, but specially for Edge Processing and memories, Edge Sensing and Imaging, Edge Communication and Edge Power Management. The proposed solutions should start at TRL 1-2 and reach TRL 3-4.
The projects, supported under this Challenge are expected to address one or more of the following aspects:

- fundamental issues like heat dissipation at nanoscale that has turned out to be the most critical bottleneck in information processing covering the design of a device from the understanding of the physics and the nanoscale thermal transport at component level to circumvent the “heat valley”, selecting the materials and process solutions.
- demonstration of the potential of the developed technologies for energy savings and contained environmental footprint towards responsible smart edge devices.

The proposed developments may cover (among others):

At Design level.

- Computer modelling based on the fundamental understanding of heat transport across layers and interfaces, harvesting fluctuations instead of fighting them for computing or the use of different state variables, e.g., spins, photons, phonons or mechanical switches, instead of charge.
- Analysis of the dissipation mechanisms in signal transmission and conversion, heat removal from hot spots in components and circuits, potential for energy conversion at the nano-scale, etc.

At Materials/Process levels:

- Novel or unique electrical, mechanical and optical interconnections or other switching mechanisms
- Efficient heat dissipation new materials for in-chip heat dissipation, e.g., 2D materials
- Embedding energy harvesters in the final devices and/or circuits
- Effective 3D multi-die heterogeneous integration including advanced packaging, heterogeneous integration, and modular design of components (such as chiplets)

At Device/Architecture levels:

- Molecular electronic circuits
- Beyond CMOS. Non mainstream semiconductor transistors including a plausible circuit concept, e.g., single electron transistors.
- Novel non-von Neumman architectures and alternative processing approaches

2.3 Expected outcomes and impacts

The portfolio of projects selected under this Challenge is expected to collectively:

- derive fundamental bounds for energy consumption and designing practical and basic scenarios to minimize the energy costs of the different processes
- harness energetic efficiencies as optimization tools to operate smart technological choices to build smart edge devices.

The expected impact from this Challenge is to open an unprecedented way for the reduction of power consumption in information processing, transmitting, etc. by developing new fundamental technology solutions going from advanced materials to advanced devices and circuits, that holistically will allow a drastic reduction of energy consumption of smart edge solutions.

2.4 Specific conditions

The applicants must describe in their proposal energy-based metrics for the technologies and methodologies to measure them and establish benchmarks.
Stable, abundant and non-toxic materials which withstand device and circuit processing steps should be used.

3 Portfolio considerations for the evaluation of applications to the Challenge

This section describes how portfolio considerations will be taken into account in the second stage of the evaluation. For more details of the full evaluation process please refer to the EIC Work Programme.

3.1 Categories

Options to reduce energy usage in smart edge devices include using architectures in which memory and compute are proximate, use of low energy and low-latency interconnects like optical components, or efficient heat dissipation new materials minimizing losses due to resistance.
Energy efficiency of smart edge devices can be tackled at all levels, starting from the design and the materials up to the architectures. For optimal results and thanks to the portfolio approach, we want to take into consideration all levels.

Starting from the highest ranked proposal, the portfolio-building process will be based on the preliminary mapping by the committee of the proposals to the two following categories: application and level.

The following table summarises the categories and their components/values together with some examples:

Category	Components/Values
Applications	• Edge processing • Edge Communication • Edge Power management • Edge sensing • Others
Level	i) **Novel Nanoelectronics solutions**: Efficient heat dissipation new materials for in-chip heat dissipation, e.g., 2D materials. ii) **Circuit level:** Embedding energy harvesters in the final devices and/or circuits; analog-digital-optical integration; novel circuits based on new ultra-wide-bandgap semiconductors and combination with CMOS. iii) **Advanced packaging technologies**: Novel or unique electrical, mechanical and optical interconnections or other switching mechanisms or Effective 3D multi-die heterogeneous integration (not at SiP level). iv) **Architecture level solution:** (not at system level).

3.2 Portfolio considerations

Initially, the evaluation committee will look at different proposals under the "level" category. It is considered that one proposal addressing the Architecture level will be sufficient for the portfolio we want to build. Then we will build the remaining of the portfolio to be balanced in terms of number of proposals addressing the first three level values, while at the same time covering different applications and, looking for potential complementarities among the projects to identify a clear added value for the development of synergies and collaborations among the projects in the portfolio. The goal will be to maximise the overall impact of the portfolio on the expected outcomes and impacts of the Challenge with the assumption that results of the portfolio activities would benefit from the convergence of different research disciplines.

For example, developments in new ultra-wide-bandgap semiconductors for edge power devices could find synergies with projects delivering 3D packaging novel solutions that combined would have an important impact on the energy consumption of those devices. It could also be that those developments in new ultra-wide-bandgap semiconductors in Edge communication and substrates could be shared for devices not envisaged in the proposal.

The combination of solutions at the different levels proposed will support the overall objective of this challenge towards a drastic impact on decreasing the energy consumption of any smart edge device. The aim is also to demonstrate the potential of the In-depth understanding of the physics of fundamentally different device-working mechanisms and experimental demonstration of novel, highly energy-efficient and scalable electronic devices and to use energy efficiency as an additional design variable that bridges design space trade-offs across devices and architectures.

Consequently, this means that the projects selected for funding after the second step are expected to differ from the ranking list established from the first step (score based ranking after assessment of each proposal separately).

4 Implementation of the Challenge portfolio

Once selected, projects will be expected and obliged to work collectively during the implementation of their projects under the guidance of an EIC Programme Manager. This section summarises some of the key aspects of this pro-active management which applicants should take into account in preparing their proposals.

4.1 Proposal preparation and grant negotiations

Applicants may be requested to make amendments to their proposed project to take into account the portfolio activities. Such changes may for instance include additional tasks to undertake common/ joint activities (workshops, data exchanges, joint research, etc) with other projects in the portfolio.

Based on previous experience, it is advised to foresee in your proposal a dedicated work package for portfolio activities and to allocate at least 10 person-months (see below for the purpose and examples of such activities). You may propose concrete activities or remain generic in your description.

If you fail to do this during proposal time, your proposal will not be scored lower during the evaluation, but in case your proposal is selected for grant agreement preparation, you will be requested to add the portfolio work package to your grant agreement. Please be aware that in that case the maximum grant you receive will not change, and you will need to find the resources for portfolio activities within the foreseen project budget.

4.2 Challenge portfolio roadmap/ strategy plan

This Challenge portfolio of projects aims at:

1. deriving fundamental bounds for energy consumption and testing computational models for different heat dissipation models.
2. defining energy efficiency parameters to help in the selection of technologies and innovations to design and manufacture energy-efficient smart edge devices.
3. lowering barriers of entry by raising awareness on clear metrics for energy efficiency and implementing solutions in the appropriate software tools.
4. enhancing the commercialisation potential of the portfolio individual project, as a result of its active participation in the portfolio activities: Ensuring that portfolio members, can access the right industry partners to explore key partnerships.

In order to accomplish the above the Programme Manager needs to develop and agree on a strategy plan for the Energy-efficient Electronics portfolio with the portfolio projects. Following the selection of proposals to be funded under the Challenge, the Programme Manager will work together with the selected projects to develop a common strategy plan/roadmap for the Portfolio. This plan will integrate the activities and milestones of the individual projects into a shared set of specific objectives and cross-project activities. The roadmap serves as a common basis for implementing the projects - including possible adjustments, reorientations, or additional support to projects - and can be updated in light of emerging results or difficulties during the implementation. The objectives can be revised, for instance based on projects' unexpected achievements, new technology trends, external inputs (other projects, new calls…).

In particular, the Portfolio roadmap/ strategy plan will include activities on the transition to innovation and commercialisation, and to stimulate business opportunities. These activities may be reinforced during the implementation with additional funding and expertise through pro-active management.

Non-exhaustive examples of activities towards the above-mentioned aims are:

Technology:

- Providing access to specific research infrastructure or design tools especially in the frame of the Chips JU instruments

- Design of practical and basic scenarios to minimize the energy consumption of the different solutions in the portfolio.

- Exploring ways to infuse into the codesign process and the EDA toolchain, the potential reduction of the energy reduction at chip design level

Transition of technology to innovation

- Market analysis: Map the targeted players in a market and exchange the market research analysis results with other portfolio projects to identify specific players with which the entire portfolio can establish partnership(s) of much higher impact as opposed to that of the individual project.

- Discussions on IP, licensing and business models and commercialisation strategy

Communication and dissemination:

- Disseminate relevant outcomes of the research work of the portfolio members to the general public or to other researchers and stakeholders (EDA providers, integrators or end-users) through common activities at scientific conferences or trade-fairs.

- Effectively communicate any key outcome of the research work of the portfolio members collectively and/or an individual project, to early stage private and corporate investors focused on the same field.

These tasks require the active participation of portfolio members to a series of meetings called for and steered by the Programme Manager. Portfolio projects will be expected to exchange information on the proposed research methodologies, experimental tests, techno-economic input data and relevant results achieved, in order to collectively use the available resources. This exchange of data between portfolio members can enhance the potential of individual projects, use of results originating from the analysis of common databases, as well as their chances to establish key partnerships.

4.3 Tools though which projects can receive additional support

Projects in the portfolio may be offered additional support, either individually or collectively, in order to reinforce portfolio activities or explore the transition to innovation. Such additional support includes:

- Booster grants of up to €50k (see Annex 5 of the EIC Work Programme)
- Access to additional EIC Business Acceleration Services (see https://eic.ec.europa.eu/eic-funding-opportunities/business-acceleration-services_en)
- Access to the Fast Track to the EIC Accelerator, which would follow a project review (see Annex 3 of the EIC Work Programme)
- Interactions with relevant projects and initiatives outside the portfolio, including other EU funding initiatives as well as those supported by national, regional or other international bodies.